

SMPS MOSFET

IRFB38N20DPbF
IRFS38N20DPbF
IRFSL38N20DPbF

HEXFET® Power MOSFET

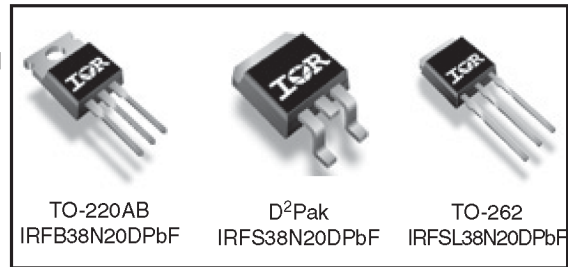
Applications

- High frequency DC-DC converters
- Plasma Display Panel
- Lead-Free

Benefits

- Low Gate-to-Drain Charge to Reduce Switching Losses
- Fully Characterized Capacitance Including Effective C_{OSS} to Simplify Design, (See App. Note AN1001)
- Fully Characterized Avalanche Voltage and Current

Key Parameters		
V_{DS}	200	V
V_{DS} (Avalanche) min.	260	V
$R_{DS(ON)}$ max @ 10V	54	m Ω
T_J max	175	$^{\circ}$ C



Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ $T_C = 25^{\circ}$ C	Continuous Drain Current, V_{GS} @ 10V ⑦	43*	A
I_D @ $T_C = 100^{\circ}$ C	Continuous Drain Current, V_{GS} @ 10V ⑦	30*	
I_{DM}	Pulsed Drain Current ①	180	
P_D @ $T_A = 25^{\circ}$ C	Power Dissipation ⑦	3.8	W
P_D @ $T_C = 25^{\circ}$ C	Power Dissipation ⑦	300*	
	Linear Derating Factor ⑦	2.0*	W/ $^{\circ}$ C
V_{GS}	Gate-to-Source Voltage	\pm 30	V
dv/dt	Peak Diode Recovery dv/dt ③	9.5	V/ns
T_J	Operating Junction and	-55 to + 175	$^{\circ}$ C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw⑥	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.47*	$^{\circ}$ C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface ⑧	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient⑨	—	62	
$R_{\theta JA}$	Junction-to-Ambient⑩	—	40	

* $R_{\theta JC}$ (end of life) for D²Pak and TO-262 = 0.50 $^{\circ}$ C/W. This is the maximum measured value after 1000 temperature cycles from -55 to 150 $^{\circ}$ C and is accounted for by the physical wearout of the die attach medium.

Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	200	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔV _{(BR)DSS/ΔT_J}	Breakdown Voltage Temp. Coefficient	—	0.22	—	V/°C	Reference to 25°C, I _D = 1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	—	0.054	Ω	V _{GS} = 10V, I _D = 26A ④
V _{GS(th)}	Gate Threshold Voltage	3.0	—	5.0	V	V _{DS} = V _{GS} , I _D = 250μA
I _{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	V _{DS} = 200V, V _{GS} = 0V
		—	—	250		V _{DS} = 160V, V _{GS} = 0V, T _J = 150°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} = 30V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} = -30V

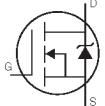
Dynamic @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
g _{fs}	Forward Transconductance	17	—	—	S	V _{DS} = 50V, I _D = 26A
Q _g	Total Gate Charge	—	60	91	nC	I _D = 26A
Q _{gs}	Gate-to-Source Charge	—	17	25		V _{DS} = 100V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	28	42		V _{GS} = 10V, ④
t _{d(on)}	Turn-On Delay Time	—	16	—	ns	V _{DD} = 100V
t _r	Rise Time	—	95	—		I _D = 26A
t _{d(off)}	Turn-Off Delay Time	—	29	—		R _G = 2.5Ω
t _f	Fall Time	—	47	—		V _{GS} = 10V ④
C _{iss}	Input Capacitance	—	2900	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	450	—		V _{DS} = 25V
C _{riss}	Reverse Transfer Capacitance	—	73	—		f = 1.0MHz
C _{oss}	Output Capacitance	—	3550	—		V _{GS} = 0V, V _{DS} = 1.0V, f = 1.0MHz
C _{oss}	Output Capacitance	—	180	—		V _{GS} = 0V, V _{DS} = 160V, f = 1.0MHz
C _{oss eff.}	Effective Output Capacitance	—	380	—		V _{GS} = 0V, V _{DS} = 0V to 160V ⑤

Avalanche Characteristics

	Parameter	Min.	Typ.	Max.	Units
E _{AS}	Single Pulse Avalanche Energy ②⑥	—	—	460	mJ
I _{AR}	Avalanche Current ①	—	—	26	A
E _{AR}	Repetitive Avalanche Energy ①	—	390	—	mJ
V _{DS (Avalanche)}	Repetitive Avalanche Voltage ①	260	—	—	V

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	44	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I _{SM}	Pulsed Source Current (Body Diode) ①⑥	—	—	180		
V _{SD}	Diode Forward Voltage	—	—	1.5	V	T _J = 25°C, I _S = 26A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	160	240	nS	T _J = 25°C, I _F = 26A
Q _{rr}	Reverse Recovery Charge	—	1.3	2.0	μC	di/dt = 100A/μs ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

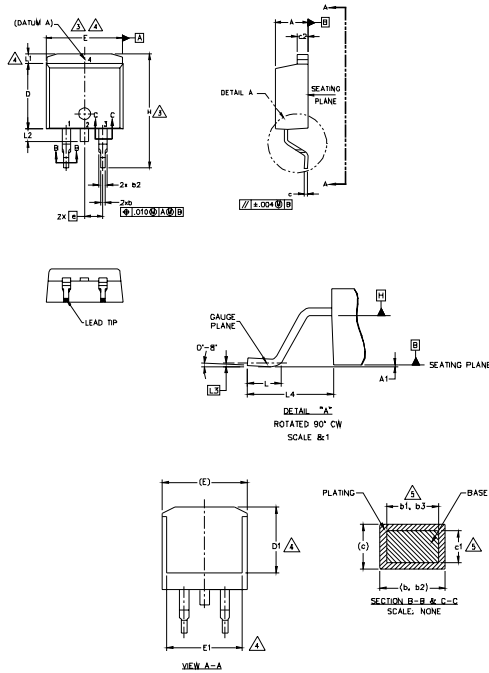
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D²Pak Package Outline

Dimensions are shown in millimeters (inches)



SYMBOL	DIMENSIONS				ZONES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	5
A1	0.00	0.254	.000	.010	
b	0.51	0.99	.020	.039	5
b1	0.51	0.89	.020	.035	
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.58	0.74	.015	.029	
c1	0.58	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	-	.270	-	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	-	.245	-	4
e	2.54	BSC	.100	BSC	4
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	
L1	-	1.65	-	.066	
L2	-	1.78	-	.070	4
L3	0.25	BSC	.010	BSC	
L4	4.78	5.28	.188	.208	

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES]
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
7. CONTROLLING DIMENSION: INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE 10-263AB.

LEAD ASSIGNMENTS

DIODES

- 1.- ANODE (TWO DIE) / OPEN (ONE DIE)
- 2.- CATHODE
- 3.- ANODE

HEXFET

- 1.- GATE
- 4.- DRAIN
- 3.- SOURCE

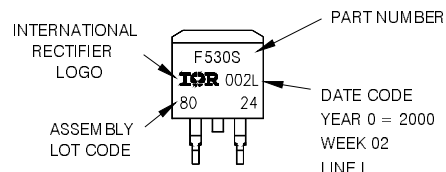
IGBTs, CoPACK

- 1.- GATE
- 2, 4.- COLLECTOR
- 3.- EMITTER

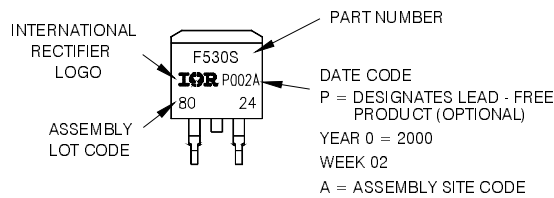
D²Pak Part Marking Information

EXAMPLE: THIS IS AN IRF530S WITH
LOT CODE 8024
ASSEMBLED ON WW 02, 2000
IN THE ASSEMBLY LINE 'L'

Note: "P" in assembly line position
indicates "Lead - Free"



OR

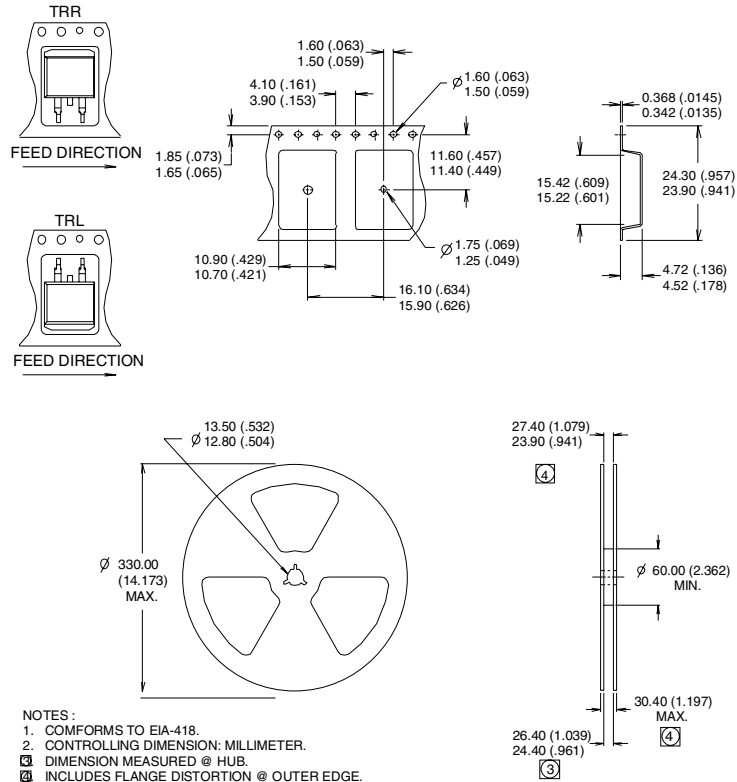


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D²Pak Tape & Reel Information



Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$, $L = 1.3\text{mH}$
 $R_G = 25\Omega$, $I_{AS} = 26\text{A}$.
- ③ $I_{SD} \leq 26\text{A}$, $di/dt \leq 390\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 175^\circ\text{C}$.
- ④ Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$.
- ⑤ C_{OSS} eff. is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑥ This is only applied to TO-220AB package.
- ⑦ This is applied to D²Pak, when mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.

Data and specifications subject to change without notice.
 This product has been designed and qualified for the Automotive [Q101] (IRFB38N20DPbF),
 & Industrial (IRFS38N20DPbF/IRFSL38N20D) market.

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